**Tutorial proposal**

**Title: Digital Electronic System on Chip (SoC) Design Methodologies – Evolution and Trends**

1. **Presenter:**

**Prof. Marcian Cirstea**

Professor and Head of School of Computing and Information Science

Anglia Ruskin University, East Road, Cambridge, CB1 1PT, United Kingdom.

Fellow IEEE, Fellow IET, Chartered Engineer UK, European Engineer (EurIng),

IEEE Industrial Electronics Society Vice-President for Planning and Development (2024-2025)

Tel. +44-1223-698184, Email: [marcian.cirstea@aru.ac.uk](mailto:marcian.cirstea@aru.ac.uk); [marcian@ieee.org](mailto:marcian@ieee.org) ;

<https://aru.ac.uk/people/marcian-cirstea>

1. **Abstract**

This tutorial reviews methodologies for modelling and design of digital electronic systems, mainly focussing on those targeting Field Programmable Gate Arrays (FPGA) as system-on-chip implementation for rapid prototyping from the same CAD environment. It starts with a review of electronics development history, then focusing on Integrated Circuits. Application Specific Integrated Circuit (ASIC) and FPGA Technologies are briefly described, along with their comparative economics and position in electronic Integrated Circuits categories in general. The top-down design methodology is presented, in the context of its use for FPGA design, and a brief comparison with Microprocessor / DSP implementation approach is given.

The approaches covered initially are based on the functional modeling and verification of complete electronic systems using Hardware Description Languages (HDLs) then targeting programmable devices - mainly FPGAs - for hardware prototyping. The main features of hardware description languages-based design approach are highlighted. More recent methods based on high level languages such as System-C, using High Level Synthesis (HLS), or schematic-based Electronic System Level (ESL) design are also reviewed, following on then to discuss the advantages of higher level languages for system-on-chip solutions development and implementation.

Some advantages of the modern approaches (using Electronic Design Automation – EDA) relate to the use of a single modelling and design environment, fast design development, short time to market, generation of a CAD platform independent model, reusability of the model / design, generation of valuable IP and high-level hardware/software design partitioning. A few case studies related to power systems control are then introduced, presented as sample applications, some of them using artificial intelligence.

Pointers for future trends / evolution of the electronic design strategies and tools are then given, including the trend / expectation of software engineers to design electronics hardware, using higher-level design languages, in the context of the Computer Engineering concept and in the framework of Concurrent Engineering. A discussion of the evolution and future trends of electronic design strategies, tools and techniques is included. The IP industry has played a major role in the development of the SoC industry and will continue to do so, with a plethora of applications such as robotics, automation, security, power electronics, electric drives, aerospace, and automotive. Current challenges of design methods and tools for SoCs, such as the growing need for accommodating multi-domain integration, lower power consumption, and higher performance versus reduced size/compact implementation, increased level of smartness, big data capacity, privacy, and security will be briefly covered. Future trends and technology enablers, including smart systems, digital twins, hardware-in-the-loop (HIL) testing, open-source EDA tools, Machine Learning / Artificial Intelligence, including Large Language Models and prompt engineering will be introduced. A conclusive statement will be presented as longer term trend - generative designs are likely to emerge on a wider scale, with the role of the engineer shifting towards the analysis and appropriate interpretation of designs generated by sophisticated CAD tools, with prompt engineering likely to bring large benefits of AI into the SoC design processes.

1. **Presenter’s biography:**

**** Marcian Cirstea received his MEng in Electrical Engineering from Transilvania University of Brasov (TUB), Romania (1990), and a PhD in Electronic/Electrical Engineering from Nottingham Trent University, UK (1996). He is a professor (since 2007) and Head of the School of Computing and Information Science, Anglia Ruskin University, Cambridge, UK, after working for De Montfort University, UK. His research interests focus on methodologies and tools for electronic systems modelling and digital controller prototyping, mainly using FPGAs. More recent interests cover System-on-Chip design, including the use of artificial intelligence. In these topics, he has co-authored over 155 peer reviewed peer-reviews papers and several books and has presented his work at various international events. He is Fellow IEEE, Fellow IET, Chartered Engineer and European Engineer. Prof. Cirstea is founder and past Chairman of the ‘Electronic Systems on Chip’ Technical Committee of IEEE Industrial Electronics Society (IES) and past Vice-President for Membership Activities in IES (2013-2016). He has also coordinated an FP6 European renewable energy project consortium. Currently (2024-25), Marcian is Vice President for Planning and Development in IEEE IES and Associate Editor for IEEE Transactions on Industrial Informatics. He has received a Doctor Honoris Causa award from TUB, Romania (2016).